

ABSTRACT OF THE DISCLOSURE

A system and method for measuring fault coverage in an integrated circuit (IC) using a stuck-at fault model is disclosed. The system includes a Device Under Test (DUT) assembly having the IC that includes at least one node, a probe and a test pattern generator and interface system. The DUT's nodes are operable to be stimulated to a stuck-at fault state when stimulated by a certain frequency of electromagnetic (EM) radiation, which fault state is operable to be discovered by a suitable test vector set.